»GREEN ICT @ FMD« – COMPETENCE CENTER FOR ECOLOGICALLY SUSTAINABLE ICT

Substrate material substitution for III-V semiconductors

A Whitepaper by "HUB 3 –Production"

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1. Summary

III/V semiconductor substrate materials like GaAs or InP are used for the production of many different optical and electronic devices. To minimize the emission of toxic As and the consumption of rare elements like Ga and In, a layer transfer technology was developed which enables the bonding of III/V heterostructures on Si wafers and the recycling of the III/V substrate materials. The applicability of these pseudo substrates was demonstrated by means of a 20 nm InGaAs high-electron-mobility-transistor technology. This enabled InGaAs amplifier ICs on silicon substrates with excellent high-frequency performance.

2. Introduction

Compared with silicon, III/V semiconductors exhibit significantly higher electron mobilities and possess direct bandgaps. For these reasons they are used in many different electronic and optical devices. Typical substrate materials used for the epitaxial growth of heterostructures for optimized device performance are indium phosphide (InP) or gallium arsenide (GaAs) wafers. GaAs is classified as a carcinogen (Carc. 1B, demonstrated in animals) and reproductive toxicant (Reprotox. 1B, demonstrated in animals) substance [1]. To make use of the superior material characteristics with minimized emission of arsenide in the environment, a substrate transfer technology was developed in the frame of the project Green ICT. Hereby only the active device heterostructure is transferred onto a silicon (Si) wafer for further processing. Additionally, this technology enables the possibility of recycling the relatively scarce Ga and In material of the wafers. The production of both metals is dominated by China and the security of supply is therefore questionable. This is all the more serious because both elements are required in a wide range of high-tech products.

For the evaluation of the substrate transfer technology not only the integrity of the transferred heterostructure but also the stability of the bond is of great importance. The bond strength has to be sufficient during all high-temperature steps needed during device processing and may not show any long-term degradation which might reduce the device lifetime. For qualification the IAF 20 nm InGaAs channel high electron mobility transistor (HEMT) technology was chosen because, on the one hand, this technology includes the maximum number of metallization and dielectric layers of any IAF technology, and on the other hand the silicon substrate in combination with the substrate transfer enables new technology features like back side gates and substrate thinning down to 25 µm, which are important for further technology scaling.

The transferred layers presented in this paper are InAlAs/InGaAs heterostructures, but in the meantime also InP and Sb-based layers were successfully transferred onto silicon substrates at IAF. The only difference is the epitaxial-grown-etch-stop layer and the wet etches used to remove the remaining substrate material after mechanical grinding and afterwards the etch stop layer.

3. Pseudo Substrate

Various technologies were developed for the bonding of wafers. The bond can be based on polymers, metals or direct material interaction [2]. They have different requirements with reference to temperature, mechanical force, ambient pressure or surface preparation. For the layer transfer a SiO_2/SiO_2 direct wafer bond was chosen. This bond can be done at room temperature, which minimizes the stress due to different temperature expansion coefficients. Additionally, no vacuum is needed and the bond has a very high strength. On the downside, direct wafer bonds require very smooth wafer surfaces and any particle on the bonding interfaces will create a circular unbound area. The InGaAs/InAlAs device heterostructure was grown by MBE on 100 mm semi-insulating GaAs wafers using a 1 µm thick metamorphic buffer for adapting the lattice constant.

3.2 Surface Preparation

For the necessary planarization of the GaAs wafer surface, PECVD-deposited SiO_2 was used. Delamination experiments showed that the bonding strength was limited by the delamination of the SiO_2 layer from the III/V semiconductor surface. Improved adhesion suitable for further device processing could be achieved by optimization of the surface pretreatment and deposition parameters. Using a chemical-mechanical polishing (CMP) process, the SiO_2 surface was planarized to a low surface roughness of less than 0.5 nm. High-resistivity 100 mm Si wafers out of the box were used as transfer substrate. Before bonding both wafers have to go through a special surface activation treatment.

3.3 Wafer Bonding

After mechanical alignment of the wafers to each other, the bonding is started in ambient atmosphere by applying pressure to the wafer center. The bonding front is then progressing from the wafer center to the wafer edge. Afterwards the bonding interface is inspected by infrared camera. Air inclusions are clearly visible as shown in Fig. 1.

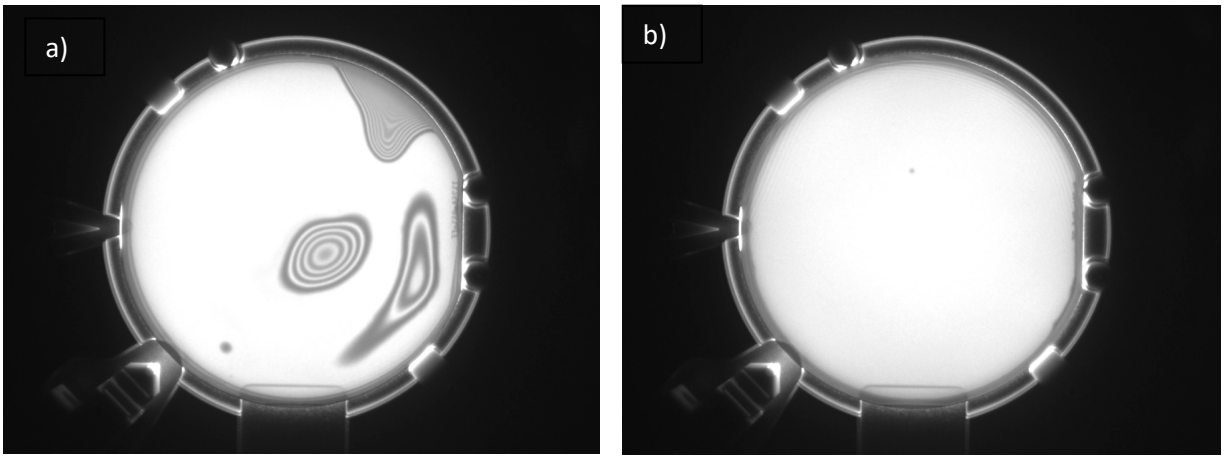

Figure 1: Infrared picture of bonded wafers with air inclusions a) and without b).

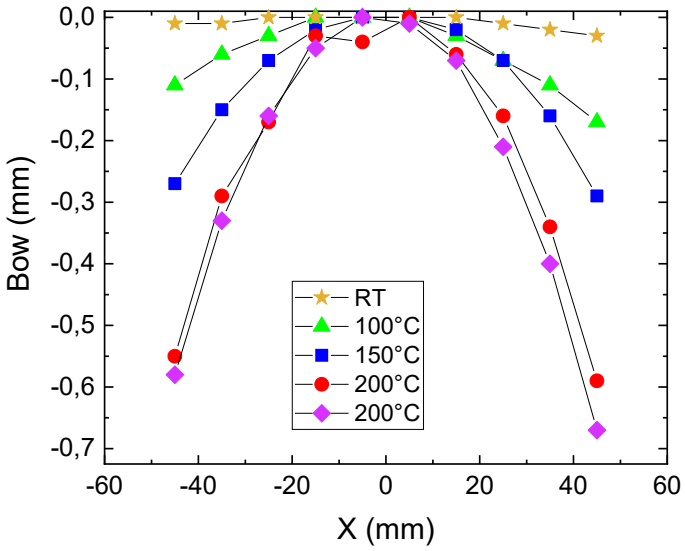

Figure 2: Bow of the wafer stack for different bonding temperatures.

The bonded GaAs / Si wafer stack is very sensitive to temperature changes due to the different temperature expansion coefficients of the materials. It is evidence of the bond's strength that, when overheated, the wafer stack shatters into thousands of pieces rather than delaminating.

We also investigated the influence of the bonding temperature on the bow of the Si/GaAs wafer stack, which gives you some possibility to tune the stress in the active device layer (Fig. 2).

3.4 III/V Substrate Removal

To avoid any degradation of the device heterostructure, the removal of the III/V semiconductor substrate is split up into mechanical wafer grinding and chemical wet-etch processes. The GaAs wafer was ground down to a thickness of 50 µm. The rest of the substrate material together with the metamorphic InGaAlAs metamorphic buffer was selectively wet-etched stopping on an epitaxial grown etch-stop layer. The etch-stop on its part was removed with a second selective wet-etch process step. Hereafter the Si wafer with the device heterostructure on top is ready for device fabrication. For the 20 nm HEMT technology presented here the heterostructure thickness was just 100 nm.

The grinding waste is filtered and can be recycled together with the precipation of the wet etch solutions. In this way the entire GaAs substrate material can be recycled. Recycling of process residues is standard in GaAs wafer fabrication [3].

Epitaxial etch stops and selective wet-etching processes for the layer transfer onto Si wafers were developed for the InGaAs/InAlAs, InP and GaSb/InAs material systems.

4. 20 nm InGaAs HEMT MMIC Technology on Silicon Substrates

For the qualification of the III/V heterostructure pseudo-substrates the 20 nm InGaAs HEMT was chosen because of its complexity and the additional benefit for this technology. During the fabrication of monolithic millimeter-wave integrated circuits (MMICs) the wafers go through many annealing steps and are exposed to many different chemicals and mechanical procedures. All of this must not cause the bond to degrade. The highest temperature during fabrication is the alloying of the ohmic contacts at 310°C. Additionally, some 200°C long-term annealing up to 10 h are needed for the polymer dielectric layers.

The 20 nm InGaAs technology includes three interconnect metal layers isolated by BCB polymer dielectric layers, thin film resistors and MIM capacitors. With the wafer bond process, we additionally added a backside gate layer for breakdown voltage improvement and threshold voltage adjustments of the transistor. The target was to overcome some of the problems due to gate-length scaling which otherwise limits the transistor performance.

The processing starts with the epitaxial growth of the metamorphic buffer, etch-stop layer and inverted device heterostructure on 100 mm GaAs substrates. The inversion of the heterostructure layer sequence is necessary due to the bonding process. Then the backside gate is defined by electron-beam lithography in lift-off technology. For the wafer bonding the gates are encapsulated in a thick SiO_2 layer which is planarized using CMP afterwards. Wafer bonding and substrate removal was done as described in section 3. The front-side processing begins with the MESA layer after which 100 nm thick III/V material only remains in the transistor and the bond pad areas. A process schematic is given in Fig.3.

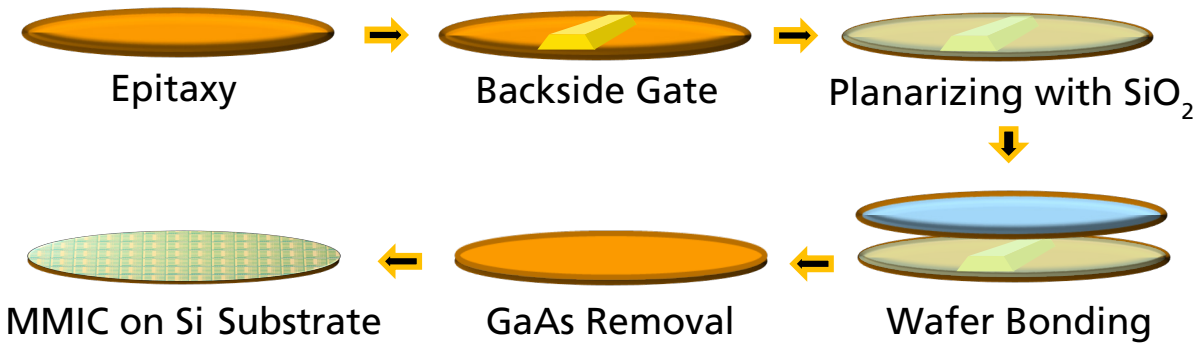

Figure 3: Schematic of the 20 nm InGaAs-on-Si process.

To suppress crosstalk within the MMIC the front-side processed silicon wafer was glued to a sapphire carrier substrate and thinned down to a thickness of 25 µm. The 20 nm InGaAs technology was developed for MMICs beyond 400 GHz. At these frequencies the 50 µm substrate thickness usually used for our InGaAs HEMT technologies is no longer sufficient. 25 µm thick GaAs MMICs proved to be very difficult to handle.

Especially picking from tape after laser dicing was impossible due to the fragility of the GaAs material. Whereas the silicon based MMICs, due to their much higher material strength could be handled in the same way as 50 µm GaAs MMICs. This is another not to underestimate advantage when using Si pseudo substrates.

4.1 Amplifier MMICs

Initial concerns about increased dissipation losses due to the higher conductivity of the silicon substrate compared to GaAs have proven unfounded, as can be demonstrated by the first noise measurements of a 600 GHz amplifier on Si substrate with only 25 µm thickness (Fig. 4). Any increased dissipation losses due to signal transmission in the circuit or within the substrate-integrated waveguide transitions would cause an increased noise level. At such high frequencies, noise measurement requires packaging the amplifier in waveguide modules. Figure 4a shows the microscope image of an amplifier packaged in split-block technology. The laser-cut waveguide transitions are integrated in the MMIC to avoid wire-bond losses which are critical at these high frequencies. Using hot–cold measurements, the amplifier module exhibited a noise figure of about 11 dB in the frequency range from 540 to 610 GHz, which also represents an outstanding value in a worldwide comparison [4].

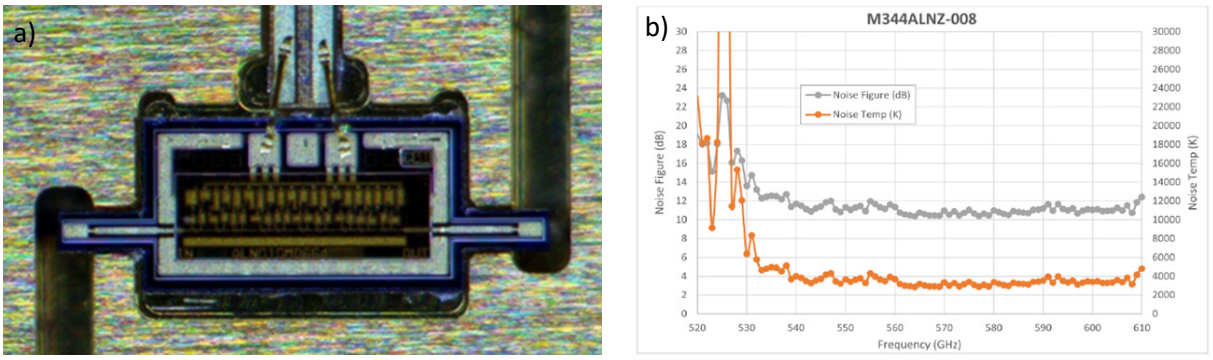

Figure 4: Microscope image of a 600 GHz amplifier with a 25 µm-thick silicon substrate a) and measured noise figure of the amplifier module in the frequency range 520–610 GHz. A very low noise figure of 11 dB was achieved.

Another demonstration of the potential given by this technology are the measured S-parameters of a 730 GHz amplifier shown in Fig. 5 with more than 30 dB small-signal gain, which outperforms any IAF GaAs substrate-based technology [5].

4.2 Backside Gate

The substrate transfer enables the integration of a backside gate into the transistor layout. This backside gate can either be used to switch between depletion or enhancement mode transistor behavior when placed directly below the frontside gate or for improving the breakdown voltage when placed between gate and drain of the transistor as shown in Fig. 6. The function of the backside gate placed between gate and

drain is to shield the gate contact from the drain potential.

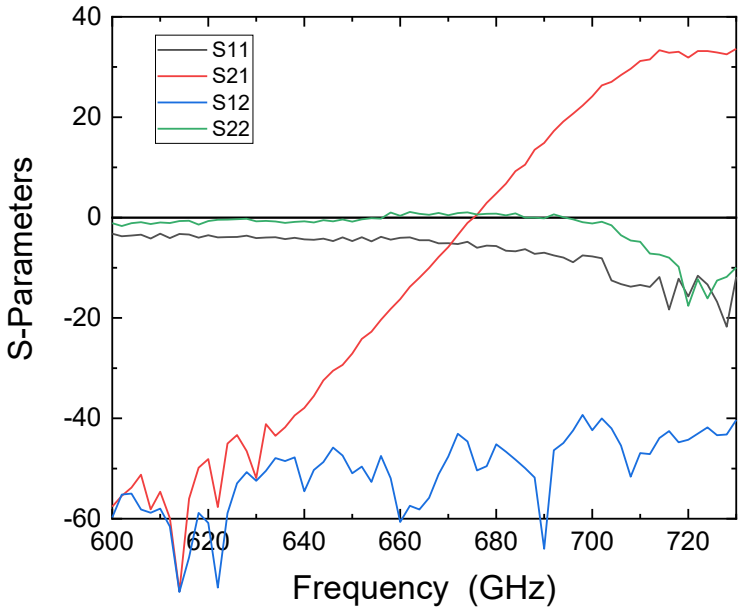

Figure 5: Measured S-parameters of a 730 GHz amplifier in 20 nm InGaAs-on-Si technology.

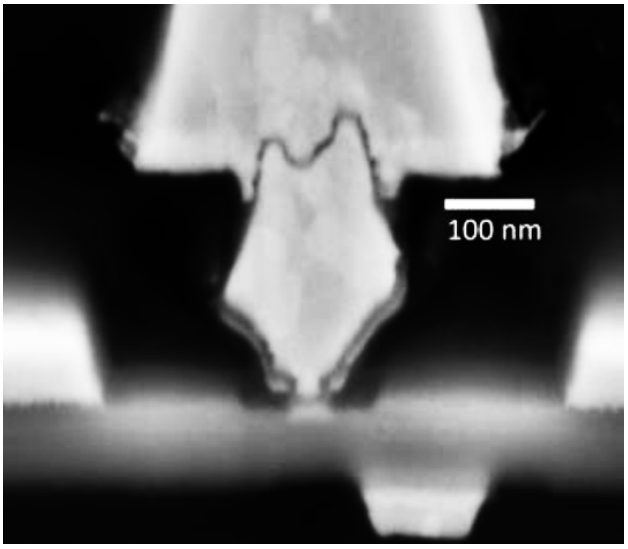

Figure 6: SEM cross section of an InGaAs-on-Si transistor with backside gate in between gate and drain contact to increase the transistor breakdown voltage.

Take away:

- The emission of toxic As can be minimized by transferring the active device III/V material layers onto Si substrates.
- This pseudo-substrate technology enables nearly 100 % recycling of the scarce by China controlled substrate materials Ga or In.
- 20 nm InGaAs HEMT amplifiers with outstanding performance demonstrate the feasibility of this technology approach.

5 Conclusion and Outlook

The transfer of InGaAs/InAlAs heterostructures grown on GaAs 100 mm substrates onto Si substrates using a SiO_2 direct wafer bond approach was successfully demonstrated. Primarily the bonding strength depended on the adhesion strength of the SiO_2 layer on the InGaAs surface. Proper surface preparation and deposition parameters were necessary. The technology can also be used for the transfer of InP- or Sb-based layers. To demonstrate the suitability of these pseudo-substrates for device fabrication 20 nm InGaAs-on-Si HEMT MMICs were processed. No degradation or delamination of the bondet III/V material during processing was observed. The realized amplifier MMICs showed outstanding high frequency performance and no reduction due to the high resistivity Si-substrate was noticed. The layer transfer approach enables the recycling of nearly 100 % of the substrate material which minimizes the emission of toxic elements like As and reduces the dependency on the import of scarce Ga or In from China.

6 Acknowledgment

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