»GREEN ICT @ FMD« – COMPETENCE CENTER FOR ECOLOGICALLY SUSTAINABLE ICT

GaN Power ICs – Components for More Sustainable ICT Power Systems

A Whitepaper by "HUB 1 –Sensor-Edge-Cloud"

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1. Summary

Many low-voltage power electronic applications are transitioning to gallium nitride (GaN)-based devices, which can increase the system's energy efficiency and power density. Within the Green ICT @ FMD project, scientists at Fraunhofer IAF investigate how gallium nitride can be used for more sustainable and resource-efficient ICT power supply systems.

2. Introduction

By 2025, the predicted amount of digital data worldwide will be 175 zettabytes (10^{21}) or 175,000,000,000 terabytes [1]. An unimaginable amount of data is growing year by year due to the advent of 5G, the growth of artificial intelligence (AI) and machine learning (ML), and that needs to be processed by information and communication (ICT) systems. As a result, increasingly powerful processors are being used, such as GPUs instead of CPUs for training AI models, which are more energy-hungry and are expected to reach a consumption per processor of 2 kW in 2030 [2]. Consequently, according to forecasts, data centers could account for up to 7% of global electricity consumption in 2030 [2]. Figure 1 shows a block diagram of power distribution or power supply system for a data center [3, 4]. As global data generation accelerates and power grid constraints tighten, the urgency for energy-efficient solutions grows — not only to reduce the environmental footprint, but also to safeguard supply reliability, particularly in data center hubs.

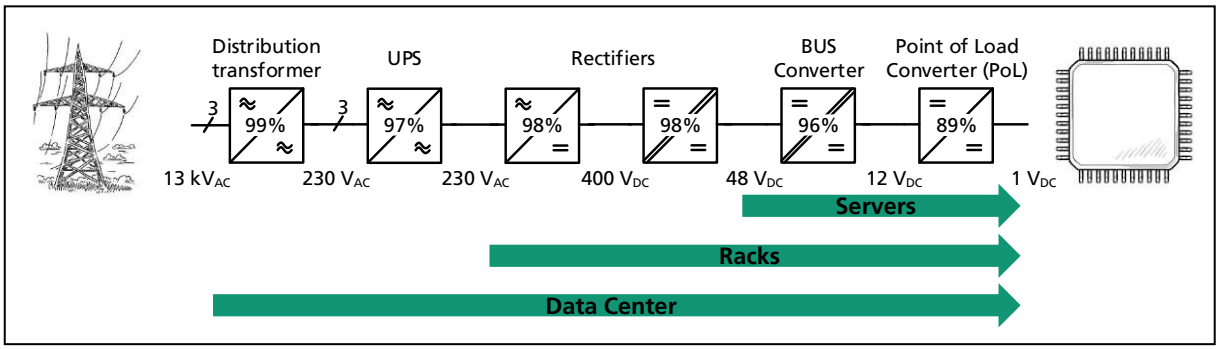


Figure 1: Block diagram of a power supply system for a data center.

But this boom in ICT systems also poses major challenges for the power supply. Why is the focus on low-voltage power conversion? There are two main reasons: First, power conversion at the lowest voltage directly touches the ICT system. This connection requires high performance of the power electronics, especially in terms of size, power density and transient response. Second, the highest conversion losses occur at low voltage – the lower the voltage, the higher the losses [3]. As illustrated in Figure 1, system losses are predominantly concentrated in the low-voltage stages — such as the bus converter and point-of-load (PoL) converter — where efficiency improvements have the greater impact. In contrast, high-voltage and high-power stages already operate at relatively high efficiencies, leaving less opportunity for energy savings. While innovations in these high-power areas may enhance power density or reduce cost, the overall energy benefit is limited. In comparison, advancements at the low-voltage end can significantly improve efficiency, cost, and power density. Moreover, gains in low-voltage efficiency cascade upstream, lowering the demands on earlier power conversion stages and thereby reducing their associated losses and costs [3].

The key components in the converters are the power semiconductors. Previously, standard semiconductor material for power devices in the low-voltage power supply of ICT systems is silicon (Si), which is increasingly being replaced by gallium nitride (GaN). GaN is a by-product of aluminum production and is processed on wafers in machines based on the established silicon technology but with fewer process steps and thus reduced energy consumption. At the same time, GaN devices can be realized on a smaller area than Si, resulting in a higher yield of chips for the same wafer size. As an example, the GaN device manufacturer Efficient Power Conversion EPC launched a GaN power transistor of the 40 V-class this year that is 1/3 the size and has half the on-resistance of the best Si MOSFET. In other words, it has an area-specific on-resistance $R_{ON}{\times}A$ of 3.6 mΩ×mm^2 compared to 9.6 mΩ×mm^2, which is one of the most important figure-of-merits (FOM) for power semiconductors. At the same time, 15 V GaN transistors (also known as high-electron mobility transistor HEMT) with $R_{ON}{\times}A$ of 2 mΩ×mm2 are to be released, which are relevant for

PoLs [5]. In terms of R_{ON}×A and the associated conduction losses per chip area, GaN is therefore advantageous for use in low-voltage power conversion. At the same time, GaN has low switching losses due to the reduced chip area compared to Si MOSFETs, which are benchmarked in the FOM R_{ON}×Q (on-resistance × gate charge Q_G, gate-drain charge Q_{GD}, or output Q_{OSS}). The faster-switching frequencies and better performance of GaN devices enable higher power densities with higher efficiencies than silicon-based converter designs.

In addition to these better FOMs, it has another property: it has a lateral device structure. This makes it possible to integrate further transistors or other active or passive components to the power transistor on chip in order to realize circuits, functions or topologies, known as GaN power integration or GaN power ICs. These GaN integration is the next step for increasing power density and higher level of integration resulting in a reded bill of material and therefore lower climate impact [6].

In this article, the simplest topology for low-voltage conversion, the non-isolated synchronous buck converter, is analyzed and optimized regarding the power semiconductors. For this purpose, the analysis is described in Section 3, which is the basis for a graphical user interface (GUI) of an application, which calculates the optimal chip area for the power transistors, the efficiency and, based on this, the CO_2 footprint with a corresponding mission profile. Section 4 shows voltage conversion case studies that can be calculated and displayed quickly and easily using the GUI. Section 5 discusses the application of the GUI and the additional possibility of GaN integration in the context of environmental considerations. Finally, Section 6 concludes this article and gives an outlook.

3. Theoretical Background

One of the most commonly used topologies in low-voltage conversion is the half-bridge (HB) consisting two power transistors in high-side (HS) and low-side (LS) configuration, see Figure 2. The half-bridge with *LC* filter known as synchronous buck converter can be used for DC-DC conversion like the bus or PoL converter.

But what is the optimum on-resistance of the power transistors in the half-bridge configuration for a given application with specific input voltage V_{IN}, output voltage V_{OUT}, switching frequency f_{SW}, etc.? Which types of losses must be taken into account? And what is the CO_2 footprint for the power devices in the application? In order to answer these questions, in the following an analysis is carried out on the basis of the synchronous buck converter.

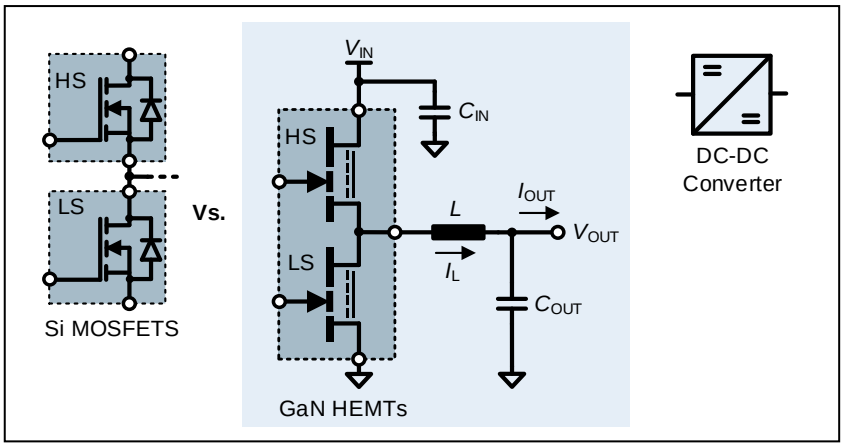


Figure 2: Non-isolated DC-DC converter as synchronous buck converter realized with GaN HEMTs or Si MOSFETs.

The calculation of the analysis was carried out with the MATLAB App Designer, which provides a GUI for the input data and the output of the data as well as the visualization. The programming was implemented using the flowchart in Figure 3.

Input data is listed in different categories (see Figure 3):

1. Converter: input voltage V_{IN} in [V], output voltage V_{OUT} in [V], switching frequency f_{SW} in [MHz], output current $I_{OUT,min/nom/max}$ (minimal/nominal/maximal) and a step size for the visualization in [A].
2. Power semiconductor: gallium nitride or silicon, calculation with optimal on-resistance or alternatively input of values for $R_{ON,HS/LS}$ in [mΩ].
3. Losses: check boxes for the different loss types to be considered. These include conduction losses P_{COND}, switching losses P_{SW}, gate drive losses P_G, reverse recovery losses P_{QRR}, output capacitance charge losses P_{QOSS}, diode conduction losses P_{DIODE} (with input of a specific dead time in [ns]), inductor losses P_L, control losses P_{CONT} (with input of a power consumption in [mW]), and losses of the common source impedance CSI (with input of a source impedance in [pH]).
4. Passives: inductor L parameters like inductance in [nH], DC resistance in [mΩ] and average of AC losses (over output current) in [mW] and output capacitor C_{OUT} parameters like the capacitance in [µF] and equivalent series resistance ESR in [mΩ].
5. Life cycle assessment: mission profile with input of the working hours per day in [h] and as check boxes the basis of the weighted efficiency (CEC, EU, peak efficiency, or efficiency at a specific load level in [%]) and the CO_2 emission per kWh [kg×CO_{2eq}/kWh] of the electricity.
6. CO_2 footprint: manufacturing with inputs of required electricity in [kWh/cm^2], yield in [%], wafer diameter in [mm], dicing street width in [µm], climate change per wafer in [kgCO_{2eq}], surcharge in [%] as a check box if the package is included and the CO_2 emission per kWh [kg×CO_{2eq}/kWh] of the electricity.

The input data is the basis for the calculations.

Material (GaN or Si)-dependent parameters are required to calculate the optimum on-resistances and the losses. These are listed in Table 4 in the appendix. The data is taken from [7, 8].

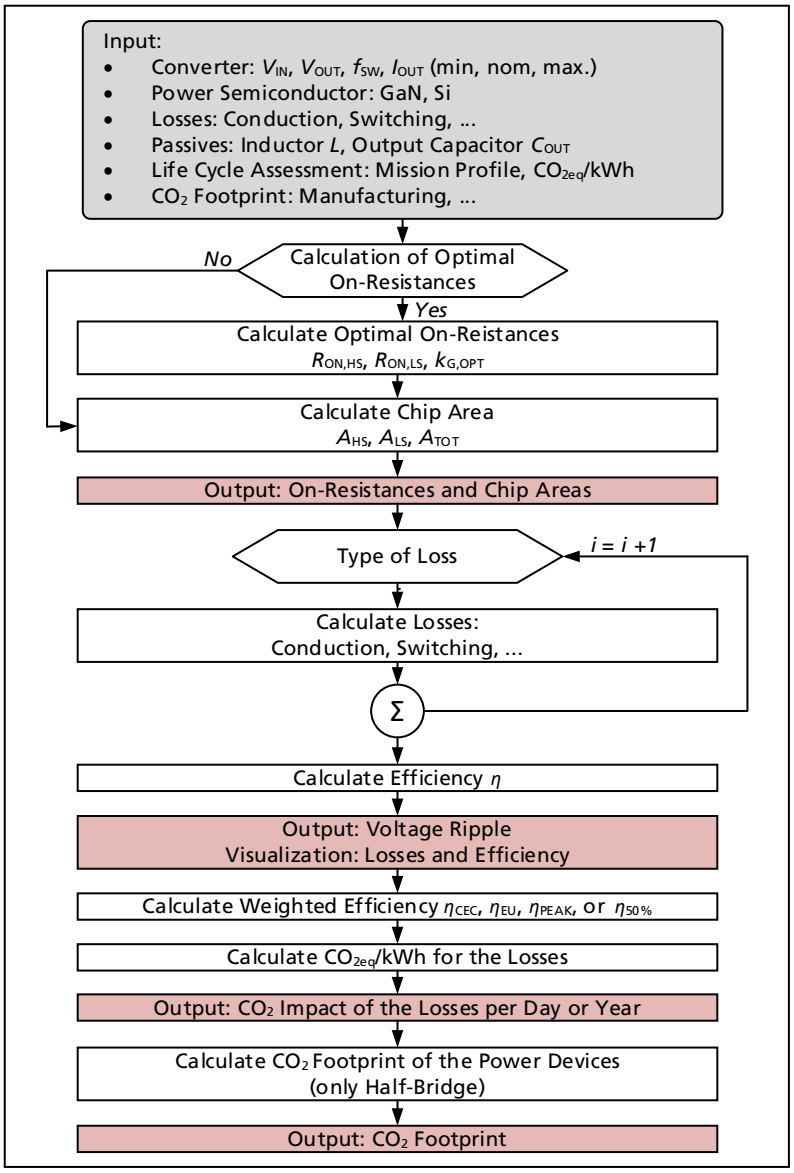


Figure 3: Flow chart of the application of the GUI.

3.1 Calculation of the Optimal On-Resistance and Die Size

The HB consists of two transistors, LS and HS transistor, as shown in Figure 2. In case of the GaN technology, these two transistors can be integrated in one die, to increase the power density and reduce parasitic inductances as well as assembly effort [9]. There is already extensive work of monolithically integrated GaN half-bridges [10], which led to the commercialization of 100 V half-bridge GaN ICs several years ago [11]. For high step-down applications, asymmetric GaN half-bridges were developed. It has also been demonstrated that monolithic GaN half-bridges can be operated at higher voltages up to 400 V [12–14]. A parameter for the HB design is the gate width ratio between the gate width of the HS and LS transistor $W_{G,HS/LS}$ given by: $k_G = W_{G,LS}/(W_{G,HS} + W_{G,LS}) = W_{G,LS}/W_{G,tot}$. The gate width is inversely proportional to the on-resistance R_{ON}, and proportional to the area of the respective transistor. One objective is to calculate the optimal on-resistances at maximizing switching device efficiency at a given load condition in the synchronous buck converter or in a general buck converter.

In many buck or boost converters a k_G = 50% (symmetric half-bridge) is used due to the same HS and LS device selection, but this is not the best choice for many conversion applications. In this context, the duty cycle *DC* of the LS conduction time during a switching period plays and important role. The duty cycle is given by $DC = V_{OUT}/V_{IN}$ for the buck converter in steady state [15] in continuous conduction mode (CCM) and critical conduction mode (CRM).

The following considerations can be made from the device losses. The conduction losses are not frequency-dependent, but the commutation losses are, which also depend on the load current. The optimum on-resistance can be calculated as follows

$$R_{\mathrm{ON,HS/LS,opt}} = \frac{1}{I_{\mathrm{OUT,nom}} \cdot \sqrt{j}} \cdot \sqrt{\left(\frac{V_{\mathrm{IN}}}{2} \cdot k \cdot Q_{\mathrm{SW,A}}\right) \cdot \left(I_{\mathrm{OUT,nom}} + \Delta I_{\mathrm{EQ}} + \Delta I_{\mathrm{EQRR}}\right) \cdot f_{\mathrm{SW}}}\ \text{[8]}, \qquad (1)$$

whereas k is a composite variable (listed in Table 4) and $j = DC$ for HS or $j = DC$-1 for LS. The derivation is explained in detail in [8]. To calculate the chip or die area, only the $R_{\mathrm{ON}} \times A$ must be divided by the $R_{\mathrm{ON,HS/LS,opt}}$: $A_{\mathrm{HS/LS}} = R_{\mathrm{ON}} \times A / R_{\mathrm{ON,HS/LS,opt}}$. An optimal on-resistance ratio can be calculated as follows $k_{\mathrm{ON,opt}} = R_{\mathrm{ON,HS}} / (R_{\mathrm{ON,HS}} + R_{\mathrm{ON,LS}})$.

Another approach is the derivation according to [9] and the calculation via the optimum gate width ratio as follows

$$k_{\mathrm{G,opt}} = \frac{\sqrt{DC - DC^2} + DC - 1}{2DC - 1}\ \text{[9]}, \qquad (2)$$

which is much simpler and does not need to include any complex parameters or normalized parameters, only the DC. The formula is simply derived from conduction losses depending on k_{G}, DC: $P_{\mathrm{COND}}(k_{\mathrm{G}}, DC)$. It is valid that $k_{\mathrm{G,opt}} = k_{\mathrm{ON,opt}}$ for DC between 20-80%! This show that consideration of the switching losses in the formula according to formula (1) does not play a role. The optimum on-resistances can also be calculated from this optimum gate width ratio $k_{\mathrm{G,opt}}$. Figure 4 shows the optimal gate width ratio $k_{\mathrm{G,opt}}$ as function of duty cycle DC. The analysis proves that the linear relationship $DC = 1\text{-}k_{\mathrm{G,opt}}$ does not apply (see Figure 4 dashed line). The optimum gate width ratio of 50% corresponds to a symmetrical half-bridge. If the converter operates with a different DC, the result is a different $k_{\mathrm{G,opt}}$. However, not only conduction losses but also switching losses have a large contribution to the total losses in a buck converter. At extreme DC between 20-80%, the relationship in equation (2) no longer applies because the max. saturation current of the smaller transistor decreases and the switching and conduction losses are affected [16].

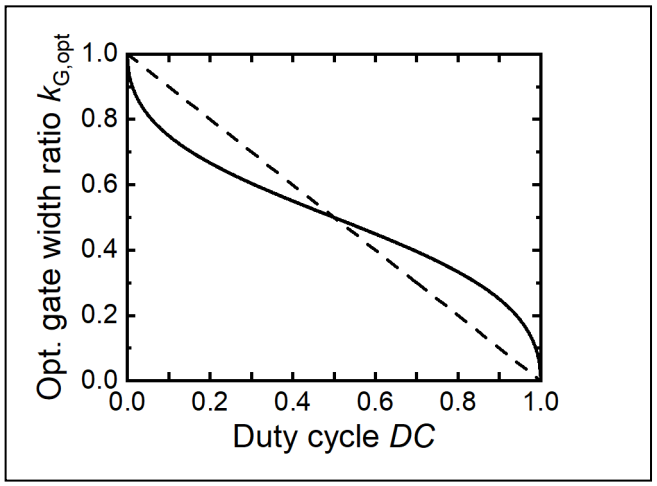


Figure 4: Optimal gate width ratio $k_{\mathrm{G,opt}}$ as function of duty cycle DC. The dashed line represents the non-valid linear relationship.

3.2 Calculation of the Losses and Efficiency of the Synchronous Buck Converter

The basis of the calculation of the losses for the synchronous buck converter is, that it is operated at hard-switching mode. In the context of the synchronous buck converter, the HS transistor is also called the control switch and the LS synchronous rectifier. The operating case of CCM or CRM therefore applies. GaN transistors largely exhibit behavior similar to that of Si-based devices, allowing them to be assessed using comparable performance metrics. Because of this similarity, GaN transistors can be optimized in a manner akin to Si MOSFETs—by balancing static and dynamic losses through appropriate die sizing. Static losses refer to components that remain unaffected by switching frequency, whereas dynamic losses are highly dependent on it. It is generally assumed that while all device parameters scale with die size, the device FOMs ($R_{\mathrm{ON}} \times A$, $R_{\mathrm{ON}} \times Q$, …) remain constant. Although the specific application may vary, the key loss components can be easily; only their relative contributions change based on the application and operating frequency.

However, for GaN power transistors, the proportions of these loss components differ from those in Si MOSFETs, leading to different optimal die size selections. To gain a deeper understanding, we begin by breaking down the total power transistor losses as follows

$$P_{\mathrm{Loss,tot}} = P_{\mathrm{COND}} + P_{\mathrm{SW}} + P_{\mathrm{G}} + P_{\mathrm{QRR}} + P_{\mathrm{QOSS}} + P_{\mathrm{DIODE}} + P_{\mathrm{L}} + P_{\mathrm{CONT}}\ \text{[15]}, \tag{3}$$

whereby the common source inductance CSI can also be taken into account in the switching losses.

In order to calculate the conduction losses P_{COND}, a ripple of the inductor current ΔI_{L} must first be calculated, which depends on the conversion ratio V_{IN}-V_{OUT}, the turn-on ratio DC and the switching frequency f_{SW} as well as the inductance L as follows

$$\Delta I_{\mathrm{L}} = \frac{(V_{\mathrm{IN}} - V_{\mathrm{OUT}}) \cdot DC}{f_{\mathrm{SW}} \cdot L}\ \text{[15]}. \tag{4}$$

With the ripple inductor current, a turn-on/off inductor current $I_{\mathrm{L,ON/OFF}} = I_{\mathrm{OUT}} \pm \Delta I_{\mathrm{L}}/2$ can be determined, which are required for the calculation of the switching losses. With ΔI_{L}, the ripple of the output voltage ΔV_{OUT} at nom. output current $I_{\mathrm{OUT,nom}}$ can be calculated as follows

$$\Delta V_{\mathrm{OUT}} = \sqrt{\left(\frac{\Delta I_L}{8 \cdot C_{\mathrm{OUT}} \cdot f_{\mathrm{SW}}}\right)^2 + (\Delta I_L \cdot \mathrm{ESR})^2}\ \text{[15]}. \tag{5}$$

Also, with the ΔI_{L}, the conduction losses for HS/LS can be calculated as follows

$$P_{\mathrm{COND,HS/LS}} = \left(I_{\mathrm{OUT}}^2 + \frac{I_{\mathrm{OUT}}^2}{12}\right) \cdot R_{\mathrm{ON,HS/LS}} \cdot j\ \text{[15]}, \tag{6}$$

whereas $j = DC$ for HS or $j = DC\text{-}1$ for LS. The conduction losses P_{COND} result from the sum of HS and LS conduction losses.

The switching losses P_{SW} can be calculated using idealized waveforms for turn-on and turn-off processes as shown in Figure 5.

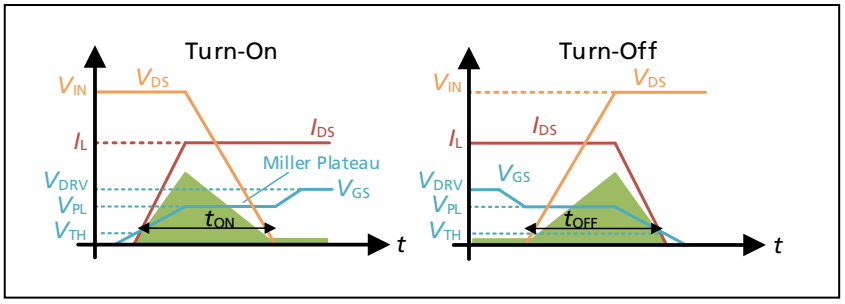


Figure 5: Idealized switching waveforms used for calculating switching loss for turn-on and -off process.

If the effect of CSI is ignored, this cannot lead to accurate loss predictions. The CSI must be determined using the parametric extraction simulation program and provides an additional resistive contribution R_{CSI} which is added to the gate resistance R_{G}. For this, the transconductance $g_{\mathrm{m}} = (2\ I_{\mathrm{OUT}})/(V_{\mathrm{PL}}\text{-}V_{\mathrm{TH}})$ and gate-source capacitance $C_{\mathrm{GS,HS/LS}} = Q_{\mathrm{GS2,A}}/(R_{\mathrm{ON,HS/LS}} \cdot V_{\mathrm{PL}})$ must be calculated, which leads to the equivalent CIS impedance R_{CIS} as follows.

$$R_{\mathrm{CSI,HS/LS}} = \frac{L_S \cdot g_m}{C_{\mathrm{GS,HS/LS}}}\ \text{[15]}. \tag{7}$$

All the parameters required to determine the switching losses for both transistors have now been calculated. Taking CSI into account, the following formulas result (details can be found in [15]):

$$P_{\mathrm{SW,ON,HS/LS}} = \frac{V_{\mathrm{IN}} \cdot I_{\mathrm{L,ON/OFF}} \cdot f_{\mathrm{SW}}}{2} \cdot \left(\frac{Q_{\mathrm{GD,A}} \cdot R_{\mathrm{G,ON}}}{R_{\mathrm{ON,HS/LS}} \cdot (V_{\mathrm{DRV}} - V_{\mathrm{PL}})} + \frac{Q_{\mathrm{GS2,A}} \cdot (R_{\mathrm{G,ON}} + R_{\mathrm{CSI,HS/LS}})}{R_{\mathrm{ON,HS/LS}} \cdot \left(V_{\mathrm{DRV}} - \left(\frac{V_{\mathrm{PL}} + V_{\mathrm{TH}}}{2}\right)\right)}\right),$$

$$P_{\mathrm{SW,OFF,HS/LS}} = \frac{V_{\mathrm{IN}} \cdot I_{\mathrm{L,ON/OFF}} \cdot f_{\mathrm{SW}}}{2} \cdot \left(\frac{Q_{\mathrm{GD,A}} \cdot R_{\mathrm{G,OFF}}}{R_{\mathrm{ON,HS/LS}} \cdot V_{PL}} + \frac{Q_{\mathrm{GS2,A}} \cdot (R_{\mathrm{G,OFF}} + R_{\mathrm{CSI,HS/LS}})}{R_{\mathrm{ON,HS/LS}} \cdot \left(\frac{V_{\mathrm{PL}} + V_{\mathrm{TH}}}{2}\right)}\right)\ \text{[15]}. \tag{8}$$

If CSI is not to be taken into account, the impedance $R_{CIS,HS/LS}$ can be set to zero accordingly. The sum of the switching losses $P_{SW,HS/LS}$ for both transistors and the total switching losses P_{SW} can now be calculated from the turn-on and turn-off parts.

Another type of loss is gate drive losses P_G, which can make a significant contribution, particularly at high switching frequencies. These losses can be calculated as follows

$$P_{G,HS/LS} = \frac{Q_{G,A}}{R_{ON,HS/LS}} \cdot V_{DRV} \cdot f_{SW} \quad [15]. \tag{9}$$

The sum can again be calculated from the parts for HS and LS.

A further loss part is the reverse recovery losses P_{QRR}. For GaN transistors, the reverse recovery charge Q_{RSS} is almost zero (see Table 4), but not for Si MOSFETs, which is why it must also be taken into account. The losses can be calculated as follows

$$P_{QRSS,HS/LS} = \frac{Q_{RSS,A}}{R_{ON,HS/LS}} \cdot V_{IN} \cdot f_{SW} \quad [15]. \tag{10}$$

The sum can again be calculated from the parts for HS and LS.

The output capacitance losses P_{QOSS} are only dependent on the input voltage. In the output capacitance C_{OSS}, an energy is stored that must be taken into account and is therefore drain-source V_{DS} or V_{IN} dependent. The losses are calculated as follows

$$P_{QOSS,HS/LS} = \frac{Q_{OSS,A}}{R_{ON,HS/LS}} \cdot V_{IN} \cdot f_{SW} \quad [15]. \tag{11}$$

The sum of both transistor parts can also be calculated here.

Only the LS transistor or synchronous rectifier in the buck converter incurs diode conduction, which is a function of the effective dead time. For both cases the diode conduction time can be calculated: for turn-off (falling of switch-node voltage) the time $t_{FALL} = (Q_{OSS,A}/R_{ON,LS})/I_{L,OFF}$ can be calculated and for turn-on (rising of switch-node voltage) the diode conduction time $t_{DIODE} = t_{DEAD}$-t_{FALL} can be calculated. These losses can then be calculated as follows

$$P_{DIODE,ON/OFF} = V_F \cdot I_{L,ON/OFF} \cdot t_{DEAD/DIODE} \cdot f_{SW} \quad [15]. \tag{12}$$

The sum here consists of the parts of the turn-on and turn-off process.

Another component in the synchronous buck converter that causes losses besides the power transistors is the inductor L. The DC and AC losses play a role here and can be calculated as follows

$$P_L = I_{OUT}^2 \cdot DCR + P_{AC,AV} \quad [15], \tag{13}$$

whereas DCR is the DC resistance and $P_{AC,AV}$ is the average AC losses of the inductor with a specific operation point of the output current range. The AC losses are dependent of the ripple current ΔI_L and also of the core losses. Some manufacturer of power inductors provides a calculator for AC and/or core losses.

The last portion of losses that are taken into account are the losses due to the control P_{COND}, which can be specified as a value.

The sum of the losses can be calculated and also split into HS and LS transistor. Using the output power $P_{OUT} = I_{OUT} \cdot V_{OUT}$, the efficiency $\eta = P_{OUT}/(P_{OUT}+P_{LOSS,tot})$ can be calculated (see Figure 3). Weighted efficiencies can be calculated on the basis of the efficiency, which are used to calculate the CO_2 emission caused by the losses. Two different weighted efficiencies can be calculated in the application, which are developed for inverters: the CEC (California Energy Commission) η_{CEC} and European average η_{EU} (see Table 5 from [17]). Alternatively, a specific load level (as example at 50% $\eta_{50\%}$) or the peak efficiency η_{PEAK} can be defined for the calculation of CO_2 emission per kWh of the converter losses.

3.3 CO_2 Impacts

A simple life cycle assessment (LCA), which considers only the usage phase, can also be performed with the application. The basis is a simple mission profile with inputs of the converter's operating hours, the weighted efficiency, and a value of the CO_2 emission in [kg×CO_{2eq}/kWh] for the electricity mix, which is highly country-dependent. The value in 2024 for Germany was 0.363 kg×CO_{2eq}/kWh [18]. Using the weighted efficiency and the nominal output power, the CO_2 emission in [kg×CO2eq/kWh] for the losses per day or per year are calculated.

Furthermore, the CO_2 footprint of the power device can be determined using the chip/die area, which was optimized in Section 3.1. In addition to the CO_2 emissions of the electricity mix (in [kg×CO2eq/kWh]), further production-dependent parameters are required for manufacturing of the devices. The country of use of the DC-DC converter does not have to correspond to the country of manufacture of the semiconductors, which means that the electricity mixes and CO_2 emissions can be different. A cradle-to-gate LCA of GaN power semiconductors was performed in [19], from which the production-dependent parameters were taken. This includes the required electricity for the production machines in [kWh/cm²], the yield of the wafer in [%], der wafer diameter in [mm], the dicing street width in [µm], because this area cannot be used, climate change per wafer in [kg×CO2eq/kWh], and a surcharge in [%] if the package should be considered. Typical values are given in the Table 5 based on [19, 20]. The value of the climate change per wafer, is a value for the resources use of minerals, metals, etc. An comparison between an Si-based and GaN-based converter is also be presented in [6].

4. Case Studies on Voltage Conversion Scenarios

In Section 3, the basis and analysis for calculating losses, efficiency, and finally, CO_2 emissions and footprint were laid. This analysis was implemented in an application and GUI using the MATLAB app design. Figure 6 shows a screenshot of the GUI. The application has more than 1500 lines of code. This application can be used to quickly calculate and compare many different voltage conversions scenarios and the two types of GaN vs. Si power transistors.

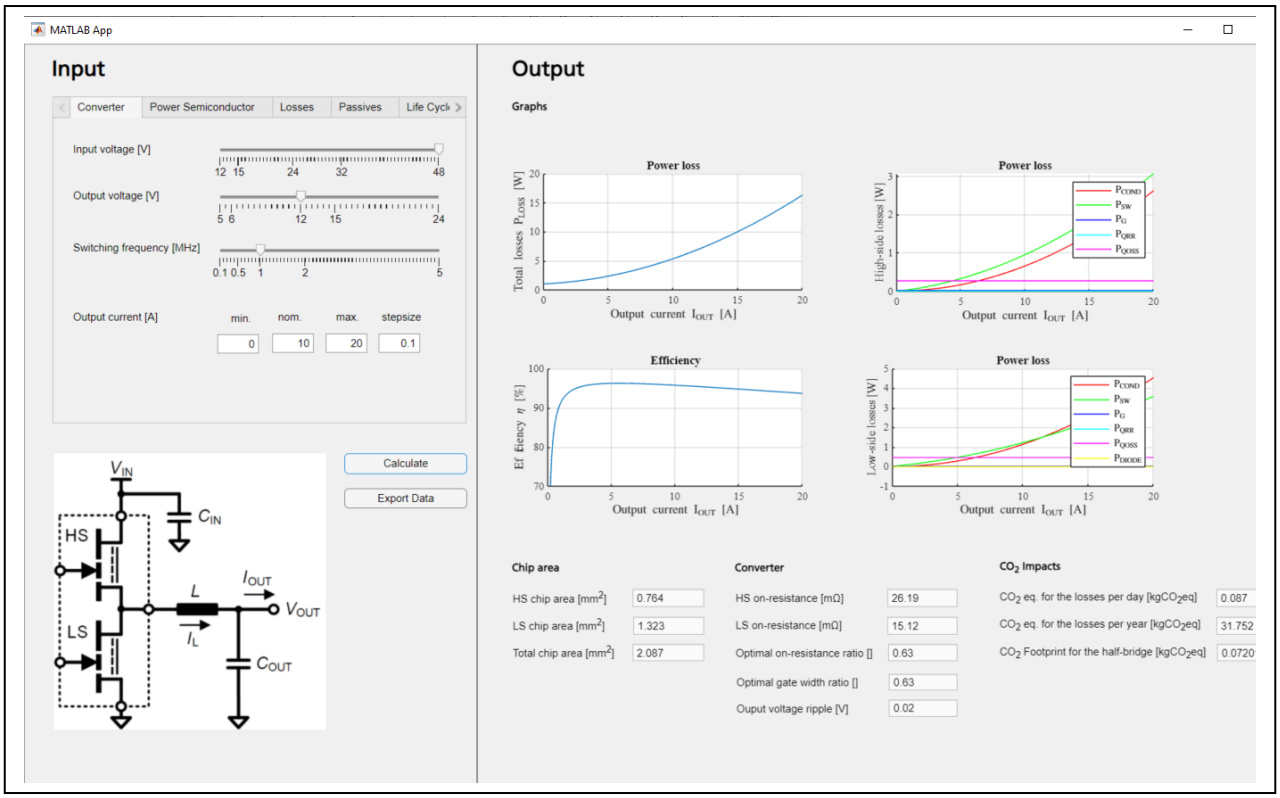


Figure 6: Screenshot of the GUI, which is implemented with the MATLAB app designer.

At this point a concrete comparison is carried out with the application and the following input parameters:

1. Converter: V_{IN} = 48 V, V_{OUT} = 12 V, f_{SW} = **200 kHz and 1 MHz**, $I_{OUT,min/nom/max}$ = 0/10/20 A with a step size of 0.1 A.
2. Power semiconductor: **GaN and Si**, calculation with optimal on-resistance.
3. Losses: all type of loss included, dead time t_{DEAD} = 5 ns, control losses P_{COND} = 150 mW, common source impedance CSI with L_S = 110 pH.
4. Passives: inductor with L = 5600 nH, DCR = 3.7 mΩ, $P_{AC,AV}$ = 110 mW and output capacitor with C_{OUT} = 120 µF, ESR = 10 mΩ.
5. Life cycle assessment: 24 h working hours per day, CEC weighted efficiency, 0.354 kg×CO2eq/kWh CO_2 emission for the electricity mix.

The results for GaN and Si from the application are inserted in Table 1 for 200 kHz and Table 3 for 1 MHz. It can be seen that the better FOMs (R_{ON}×A, R_{ON}×Q) are reflected in lower on-state resistances for GaN compared to Si, with lower losses at the same time and larger chip area for Si. An important parameter in this comparison is the switching frequency. While the switching and conduction losses are balanced in GaN, the conduction losses dominate in Si. Despite the higher chip area consumption in Si, the CO_2 footprint is very similar to that of GaN and in some cases even better (e.g., at 1 MHz, see Table 3), becomes visible in the higher maturity of the technology and the associated manufacturing parameters (wafer size, yield, etc.). But the efficiency can always be higher with GaN than with Si! This results in less loss and lower CO_2 emissions over a certain mission profile. With the mission profile of 24 working hours of the converter, which is realistic for a data center, and the weighted efficiency, this results in a saving of 15/27 g×CO_{2eq} per day for 200 kHz/1 MHz, which adds up to 6.679/9.996 kg×CO_{2eq} per year for only one synchronous buck converter! It should be noted that, for example, one processor requires one corresponding PoL converter.

Take away:

- **GaN power transistors can always be more efficient than Si!**
- Chip area can also be saved with GaN.
- Higher efficiencies have a lower CO_2 impact due to the reduction of losses and therefore lower power consumption of the converter.
- Even small efficiency increases of a few percent or per mil can add up to extreme CO_{2eq} savings for a certain mission profile or sheer number of converters required.
- **The CO_2 footprint of GaN and Si is similar.**
- The efficiency decreases with increasing frequency, but at the same time the size of the passive components, especially the power inductor, shrinks, which was not considered in this LCA.

Table 1: Results of the application for GaN and Si at 200 kHz

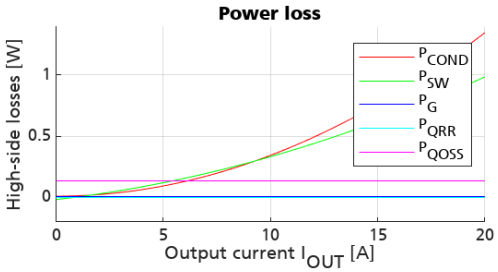
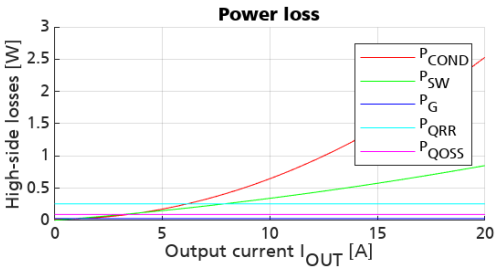
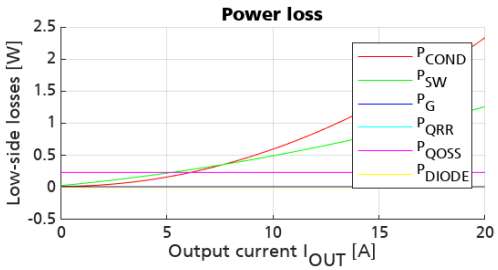
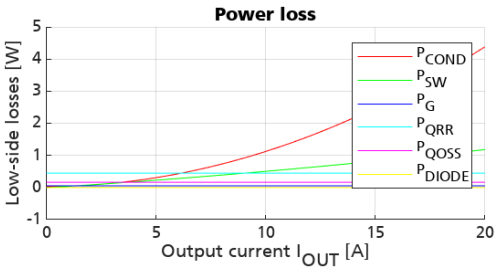
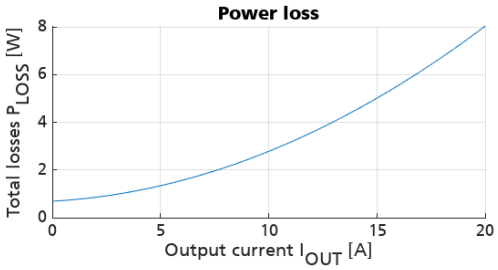
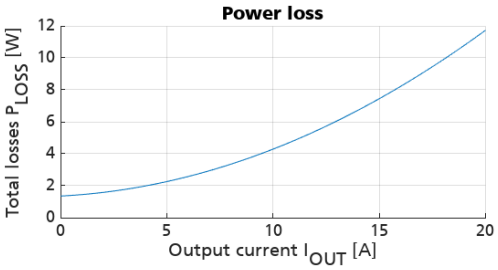
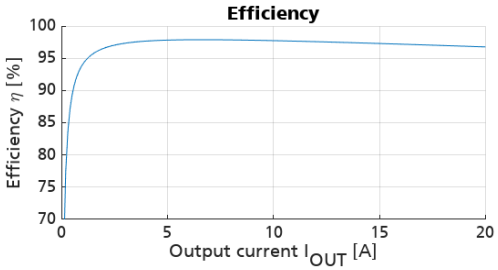
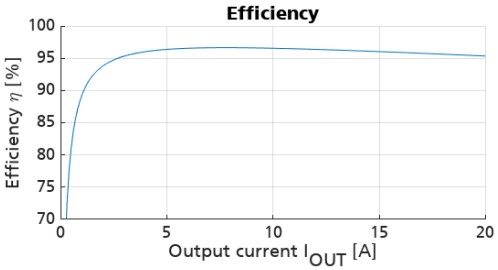
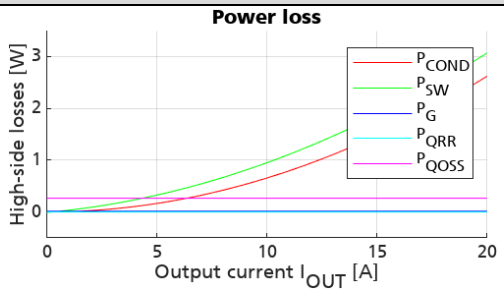
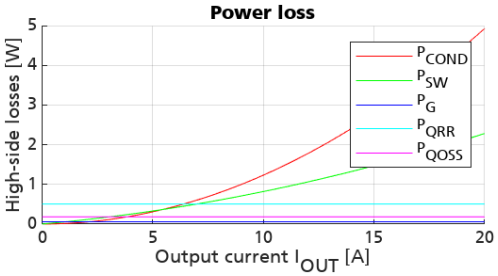
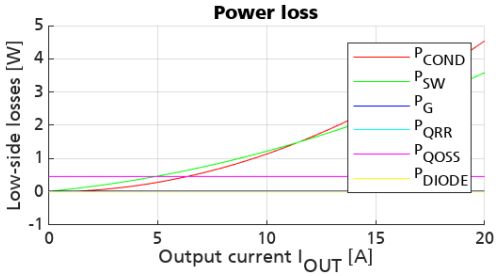
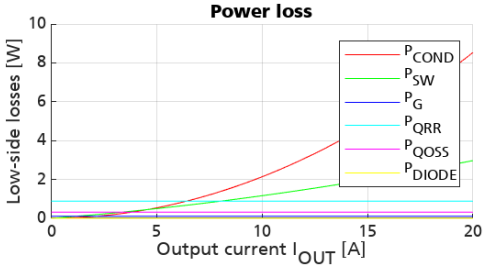
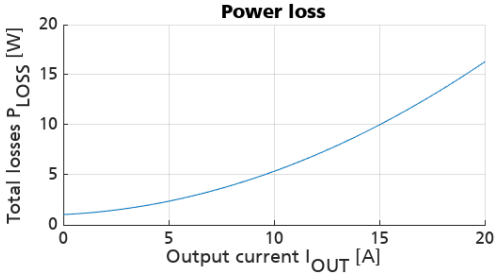
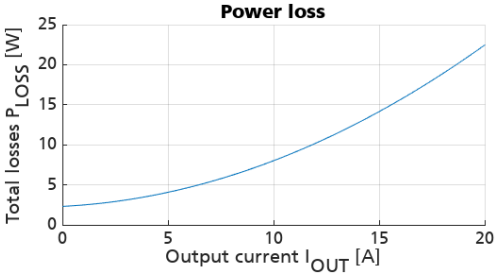
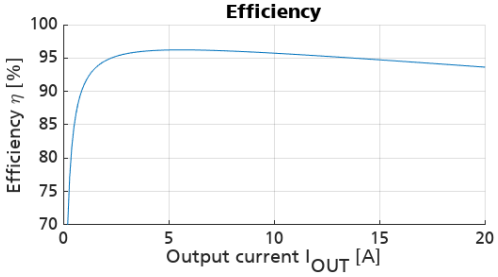
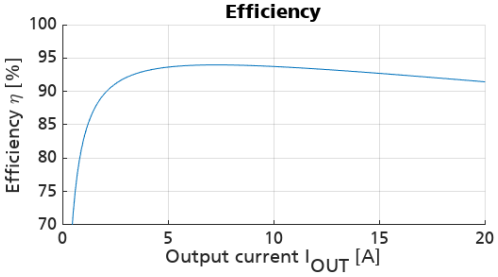
Parameter	GaN	Si
$P_{LOSS,HS}$		
$P_{LOSS,LS}$		
$P_{LOSS,tot}$		
η		
A_{HS}	1.498 mm²	2.391 mm²
A_{LS}	2.594 mm²	4.142 mm²
A_{tot}	4.092 mm²	6.533 mm²
$R_{ON,HS}$	13.35 mΩ	25.09 mΩ
$R_{ON,LS}$	7.71 mΩ	14.49 mΩ
$k_{ON,opt}$	0.63	0.63
$k_{G,opt}$	0.63	0.63
ΔV_{OUT}	0.07	0.07
kg×CO_{2eq}/day	0.070 kg×CO_{2eq}	0.085 kg×CO_{2eq}
kg×CO_{2eq}/year	**25.436 kg×CO_{2eq}**	**31.115 kg×CO_{2eq}**
CO_2 footprint	**0.1337 kg×CO_{2eq}**	**0.1447 kg×CO_{2eq}**

Table 2: Results of the application for GaN and Si at 1 MHz

Parameter	GaN	Si
$P_{LOSS,HS}$		
$P_{LOSS,LS}$		
$P_{LOSS,tot}$		
η		
A_{HS}	0.764 mm²	1.219 mm²
A_{LS}	1.323 mm²	2.112 mm²
A_{tot}	2.087 mm²	3.331 mm²
$R_{ON,HS}$	26.19 mΩ	49.21 mΩ
$R_{ON,LS}$	15.12 mΩ	28.41 mΩ
$k_{ON,opt}$	0.63	0.63
$k_{G,opt}$	0.63	0.63
ΔV_{OUT}	0.02	0.02
kg×CO_{2eq}/day	0.087 kg×CO_{2eq}	0.114 kg×CO_{2eq}
kg×CO_{2eq}/year	**31.753 kg×CO_{2eq}**	**41.749 kg×CO_{2eq}**
CO_2 footprint	**0.08101 kg×CO_{2eq}**	**0.07852 kg×CO_{2eq}**

5. Discussion

Our distinct case studies have been conducted to analyze voltage conversion scenarios using synchronous buck converters—comparing GaN and Si technologies, and switching frequencies of 200 kHz vs. 1 MHz. The results are summarized and visualized in Table 1 and Table 3. These scenarios are evaluated not only in terms of performance but also with regard to LCA considerations. Fundamentally, the methodology presented is applicable to a wide range of use cases for optimization and analysis. The key converter parameters are V_{IN}, V_{OUT}, I_{OUT}, and f_{SW}. These factors are crucial for designing the power stage or half-bridge. From a converter perspective, efficiency is the most critical performance metric, followed closely by power density, which is influenced by the load conditions and the characteristics of the passive components. In practice, regulatory energy efficiency requirements typically apply only to complete systems—such as uninterruptible power supplies (UPS), servers, and computers—but not specifically to their internal (auxiliary) DC-DC converters. Moreover, standards like CEC or EU weighted efficiency metrics, common for inverters, do not exist for DC-DC converters. Only the Energy Star® program provides minimum efficiency requirements for these devices (e.g., for rated output power ≤500 W, 70/82/89/85% efficiency at 10/20/50/100% load, respectively [21]). Consequently, peak efficiency remains a key evaluation criterion, and accurate analysis requires knowledge of the load profile, user behavior, or mission profile. In data centers, the mission profile is often calculated using the maximum output current.

Various FOMs, such as $R_{ON}\times A$, $R_{ON}\times Q$ or price$\times R_{ON}$, are used to evaluate power semiconductors and materials, as referenced in [6, 22]. These FOMs can be used to estimate conduction and switching losses. In terms of environmental impact, a key LCA consideration is the device's total CO_{2eq} emissions over its lifecycle. Both Si MOSFETs and GaN HEMTs show comparable CO_2 footprint values, although packaging—which was considered only as a surcharge—adds a significant contribution. This emission factor can be easily extrapolated by multiplying the CO_{2eq} value by the expected energy consumption (in kWh). A comprehensive LCA also includes categories such as climate change, ozone depletion, and resource usage [19]. As GaN technology continues to mature, its CO_2 footprint is expected to decrease further. Advancements in manufacturing processes, higher production volumes, and improved material utilization contribute to a lower environmental impact over time. Additionally, ongoing innovations in packaging and wafer-level integration enhance the overall efficiency and sustainability of GaN devices. This trend supports the growing adoption of GaN in applications where both performance and environmental considerations are critical. Replacing Si MOSFETs with GaN HEMTs can reduce semiconductor chip area and thereby lower CO_{2eq}. Furthermore, due to their vertical structure, Si MOSFETs require packaging, which further increases their environmental footprint. In contrast, low-voltage GaN HEMTs, with their lateral structure, enable chip-scale or flip-chip packaging, minimizing material usage. GaN's low capacitance allows for higher switching frequencies, which in turn enables smaller passive components, reducing copper usage in inductors and shrinking PCB size. Additionally, GaN-based topologies and functional integration reduce packaging and PCB area even further. This makes GaN integration an attractive option for achieving more compact, material-efficient, and environmentally sustainable power stages. As a result, 48 V GaN-based power stages are increasingly adopted in data centers and applications like drones and electric motors, where size, efficiency, and sustainability are paramount [4].

Take away:

- The CO_2 footprint of GaN could decrease further with higher maturity.
- **The lateral structure of GaN transistors allows flip-chip assembly, which has CO_2 savings compared to conventional package solutions.**
- The GaN integration of topologies and functionalities could further reduce the CO_2 footprint and impact.

6. Conclusion and Outlook

Drawing upon the analysis presented, the increasing energy demands of ICT systems, particularly within data centers, highlight the urgent need for more energy-efficient power supply solutions. Our investigation has focused on low-voltage power conversion stages, such as bus and PoL converters, where efficiency improvements offer the greatest impact due to high conversion losses. GaN power ICs emerge as a superior alternative to traditional Si for these applications. GaN devices exhibit better performance FOMs, leading to higher energy efficiency through lower conduction and switching losses. This enhanced efficiency directly translates into significant CO_{2eq} savings over the operational lifetime of the converter, which is critical for long-running applications like data centers. Even small efficiency gains accumulate into substantial CO_{2eq} reductions for numerous converters. While the manufacturing CO_2 footprint is currently similar to Si, it is expected to improve as GaN technology matures. Furthermore, GaN's lateral structure facilitates GaN power integration and enables compact designs with potentially reduced material usage by minimizing packaging and PCB area. In summary, GaN power ICs offer crucial advantages in terms of efficiency and operational CO_2 emissions, positioning them as essential components for building more sustainable ICT power systems.

As GaN technology continues to mature, its environmental impact is expected to improve further—not only due to more efficient semiconductor fabrication but also through increased levels of functional integration. However, to fully assess the life cycle advantages of GaN-based converters, a more comprehensive LCA is needed—one that includes all components within the power converter system, such as inductors, capacitors, packaging materials, and the PCB. Higher switching frequencies enabled by GaN may reduce the size and material use of passive components, but these trade-offs must be quantified holistically. Future studies should therefore focus on the system-level environmental footprint of integrated GaN solutions, considering both direct (e.g., chip and packaging) and indirect (e.g., reduced copper, smaller form factor) contributions to sustainability.

7. Acknowledgment

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8. Appendix

Table 3: Material-dependent parameters for the calculation of the optimal on-resistances and the losses. The data is taken from [7,8].

Parameter	Description	Unit	GaN	Si
$R_{ON}\times A$	Area specific on-resistance [1]	[mΩ×mm²]	20	60
$R_{ON}\times Q$	On-resistance times gate charge [1]	[mΩ×nC]	30	180
$Q_{GS2,A}$	Gate charge between device threshold and plateau voltage per normalized die area @rated I_{DS}	[pC/Ω]	7	35
$Q_{GD,A}$	Miller charge per normalized die area @V_{IN}	[pC/Ω]	21	55
$Q_{G,A}$	Total normalized gate charge @5 V rated V_{DRV}	[pC/Ω]	73	290
$Q_{OSS,A}$	Total normalized device output charge @V_{IN}	[pC/Ω]	290	375
$Q_{RSS,A}$	Total normalized device diode reverse recovery charge @rated I_S	[pC/Ω]	0	520
$Q_{SW,A}$	Total normalized switching charge from reaching threshold to end of plateau [1]	[pC/Ω]	28	90
V_{TH}	Gate-source threshold voltage	[V]	1.4	3.0
V_{PL}	Plateau voltage @rated I_{DS}	[V]	2.3	4.6
V_F	Forward drop @ rated I_{DS}	[V]	2.3	0.9
V_{DRV}	Drive voltage	[V]	5	10
$R_{G,ON}$	Gate resistance for turn-on	[Ω]	2.6	3
$R_{G,OFF}$	Gate resistance for turn-off	[Ω]	1.1	2.5
k_{ON}	$R_G/(V_{DRV}-V_{PL})$; composite variable	[1/A]	0.963	0.556
k_{OFF}	R_G/V_{PL}; composite variable	[1/A]	0.478	0.544

k	$k_{ON}+k_{OFF}$; composite variable	[1/A]	1.441	1.099
ΔI_{EQ}	Composite variable [1]	[A]	7.7	5
ΔI_{EQRR}	Composite variable [1]	[A]	0	10.5

[1] @ 100 V for GaN, @ 80 V for Si

Table 4: Calculation or composition of the weighted efficiencies [17].

Weighted Efficiency	$\eta_{5\%}$	$\eta_{10\%}$	$\eta_{20\%}$	$\eta_{30\%}$	$\eta_{50\%}$	$\eta_{75\%}$	$\eta_{100\%}$
η_{CEC}	-	0.04	0.05	0.12	0.21	0.53	0.05
η_{EU}	0.03	0.06	0.13	0.10	0.48	-	0.20

Table 5: Typical values for the manufacturing of GaN and Si power transistors [19,20].

Parameter	Unit	GaN	Si
Required electricity	[kWh/cm^2]	2	2.54
Yield	[%]	90	90
Wafer diameter	[mm]	200	300
Dicing street width	[µm]	100	100
Climate change per wafer	[kg×CO2eq/kWh]	600	600
Surcharge (Package)	[%]	20	20

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